Amendments To The Claims

The listing of claims presented below will replace all prior versions, and listings, of claims in the application.

Listing of claims:

1. (**currently amended**) A method for fabricating a semiconductor device, which comprises the steps of:

forming a gate line on a semiconductor substrate;

forming junction regions in the semiconductor substrate at both sides of the gate line;

forming and selectively removing an interlayer insulting film on the resulting substrate to form contact holes exposing the junction regions;

forming plugs in the contact holes**, wherein no annealing process is performed prior to the current step of forming the plugs in the contact holes**; and

implanting impurity ions into the plugs; and

annealing the junction regions.

2. (original) The method of Claim 1, wherein the step of annealing the junction regions is conducted by a rapid thermal annealing (RTA) process.

3. (original) The method of Claim 1, wherein the step of implanting the impurity ions into the plugs is performed after the step of annealing the junction regions.

4. (original) The method of Claim 3, which additionally comprises the step of performing a furnace annealing process after the step of implanting the impurity ions.

5. (original) The method of Claim 4, wherein the furnace annealing process is performed at a temperature of 600-900 °C.

6. (original) The method of Claim 1 or 3, wherein the step of implanting the impurity ions into the plugs is carried out using phosphorus (P) or arsenic (As) source gas at an ion implantation energy of 1040 KeV and a dose of 1.0E15-1.0E16.

7. (original) The method of Claim 1 or 3, wherein the step of annealing the junction regions is carried out at a temperature of 850-1,100 °C, a ramp-up rate of 10-200 °C/s and a ramp-down rate of 10-200 °C/s for 10-60 sec under a gas atmosphere of N_2, O_2, N_2/O_2 mixture, Ar, NH_3 or N_2O.

8. (original) The method of Claim 1, which additionally comprises the step of forming an oxide film or a nitride film on the plugs.

9. (original) The method of Claim 1 or 8, which additionally comprises the step of performing an etchback process or a CMP process on the plugs.

10. (original) The method of Claim 8, wherein the step of implanting the impurity ions into the plugs is carried out using phosphorous (P) or arsenic (As) source gas at an ion implantation energy of 10-80 KeV and a dose of 1.0E15-1.0E16.